# MODELING OF SOLDER JOINT DEFECTS THROUGH A LEVEL-SET APPROACH

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**Abstract.** Due to the inherent nature of flip-chip assembly, the solder joints lie beneath the device and therefore are not amenable to visual inspection. Hence, it is important at the design stage to ensure that solder defects such as joint separation or joint shortening do not occur in the assembly. As a first step, the solder joint is modeled using a level-set approach. Unlike conventional front-tracking approaches, the levelset method handles complicated profiles arising from merger/separation of solder joints naturally without user intervention. The model was established to determine the upper and lower limit on optimal solder volume as a function of a specific assembly configuration and is used to avoid such defects.

**Key Words.** levelset, solder-joint, flip-chip.

## 1. Introduction

Flip-chip/BGA assembly is gaining increasing importance in electronic packaging due to the area array nature of assembly, providing an option for high I/O assembly, a smaller foot print to accommodate a larger number of I/O in a smaller area, and gang-bonding to achieve multiple assembly simultaneously. However, these advantages come with a price. Due to the inherent nature of the flip-chip assembly, the solder joints lying beneath the device are not amenable to visual inspection and subsequent repair because of the obvious difficulty in visual inspection in establishing a defect free assembly. Some of the inspection approach is used for flip-chip application are: backside thinning coupled with metallization illumination [1], characterization through acoustic microscopy [10, 19], and the use of x-ray [23]. Even with these techniques, it is often very difficult to determine some of the solder defects such as necking/separation of a joint. As a result, assembly with a joint defect can be known only after the fact with hardly any option to rectify it. Therefore, it is important at the design stage to ensure that such defect do not occur in the assembly. The typical sources of solder defect in flip-chip/BGA assembly can be broadly placed in two categories (1) not enough solder at a specific site - resulting in lack of joint formation and (2) too much solder at a site - resulting in shortening of neighboring joints. The effect of solder volume is magnified by other process variables such as placement accuracy. These defects occur due to various designing and processing constraints. For example, the designer tends to specify the cylindrical/hour-glass shape for solder joint design in order to reduce stress in the joint and improve its fatigue life. This is created by using a spacer to create a

required gap between the chip and substrate [12]. However, controlling the gap is very difficult. This difficulty is compounded by the board deformation that takes place during reflow [14] and the volume distribution and constraint on placement accuracy [13]. Therefore in such a case, it is important to understand the acceptable limits on the gap as a function of design and manufacturing constraints. Reviewing existing models [7, 8, 18, 17, 11], shows that all of the model are designed to address ideal or successful joint formation. Heinrich et al.[9] presented non-dimensional profiles for avoiding solder defects and Singler and Zhang [20] [modeled the solder bridging problem using SURFACE EVOLVER]. Goldmann[5] developed physical model and heuristic equations to describe separation of a molten axisymmetric solder joint. In Evans and Spruck [3, 4] have rigorously described the generalized evolution(including topological changes) of hypersurfaces moving according to their mean curvature by using the notion of "viscosity solutions" of nonlinear PDE's. All these models including those based on SURFACE EVOLVER are solved using front tracking or similar approach i.e. the interface front is evaluated at each iteration. SURFACE EVOLVER, developed by Ken Brakke, represented a versatile surface profile modeler developed. It is a finite element model based on minimization of total energy. It has the ability to compute solder joint model with complicated pad geometry. However, Surface Evolver can only model only joint separation and not joint merging. Modeling of joint separation requires artificial removal of grid points from the computational domain. Thus, the goal is to develop a computational model that can address both joint separation and joint merging to simulate process defect. In this paper, a unified approach that can model both separation and merging has been proposed. It is based on an alternative approach to front tracking - namely, the Level Set Methods. As mentioned earlier, the goal is to develop the numerical technique to simulate solder joint defect due to merging and separation. Later, the model is applied to a set of specific case studies. No attempt has been made to generate a more general result associated with flip-chip solder joint. This is an issue we will address in the future.

## 2. Level-Set approach to solder profile modeling

The levelset approach was originally developed by Osher and Sethian [15]. In this method, a level-set function $\phi(\boldsymbol{x},t)$ represents the interface as the set where $\phi(\boldsymbol{x},t)= 0$ . As is by now well known, this method eliminates the problem of repositioning the points during the numerical calculation and is capable of capturing geometric properties of highly complicated boundaries including topological changes without explicitly tracking the interfaces. Also, it can easily extend to 3-dimensional problems. The key advantage of level-set approach is that, the surface merges and separates naturally (see Figure 1(b)). The basic idea behind the level-set method is embedding the moving interface to one higher dimensional set - this is the level set. What this means is following. Consider the closed moving interface $\partial\boldsymbol{\Omega}(t)$ in $I\!\!R^n$ with co-dimension one. We associate with $\boldsymbol{\Omega}(t)$ to a signed distance function $\phi(\boldsymbol{x},t)$ which is a Lipschitz continuous, satisfying:

$$(1) \quad \begin{aligned} \phi(\boldsymbol{x},t) &= 0 \quad for \quad \boldsymbol{x} \in \partial\boldsymbol{\Omega} \\ \phi(\boldsymbol{x},t) &> 0 \quad for \quad \boldsymbol{x} \in \boldsymbol{\Omega} \\ \phi(\boldsymbol{x},t) &< 0 \quad for \quad \boldsymbol{x} \in \overline{\boldsymbol{\Omega}}^c \end{aligned}$$

where $\boldsymbol{x} \in I\!\!R^n$, $t \in I\!\!R^+$ (see Figure 2). From the definition of $\phi(\boldsymbol{x},t)$, the zero level set $\{(\boldsymbol{x},t)|\phi(\boldsymbol{x},t) = 0\}$ is the interface of the moving object. This means that moving the interface is equivalent to updating the zero level set of with same

velocities of the interface. This follows that once we know the velocity of the interface, then we can calculate the new location of the interface using a level set function.

**2.1. Derivation of the governing equation.** Followings are some of the notations associated with level-set function $\phi$:

$$\boldsymbol{n} : (outward\ normal\ to\ the\ region) = -\frac{\nabla \phi}{|\nabla \phi|}$$

$$\kappa : (curvature) = \nabla \cdot \boldsymbol{n}$$

$$\partial \boldsymbol{\Omega} : (length) = \int_D \delta_\alpha(\phi)|\nabla \phi| d\boldsymbol{x}$$

$$\boldsymbol{\Omega} : (volume) = \int_D H_\alpha(\phi) d\boldsymbol{x}$$

where $H(\phi)$ is the numerical Heaviside function and $\delta_\alpha(\phi)$ is the numerical delta function.

$$(2) \qquad H_\alpha(\phi) = \begin{cases} 1 & \text{if } \phi > \alpha \\ 0 & \text{if } \phi < \alpha \\ \frac{1}{2}(1 + \frac{\phi}{\alpha} + \frac{1}{\pi}\sin(\frac{\pi\phi}{\alpha})) & \text{otherwise} \end{cases}$$

$$\delta_\alpha(\phi) = \frac{d}{d\phi}H_\alpha(\phi)$$

The governing equation representing the interface motion in our approach is given by:

$$(3) \qquad \frac{\partial \phi}{\partial t} = -\sigma(\kappa - \bar{\kappa})|\nabla \phi|$$

One can derive equation(3) for the solder joint (satisfying volume constraint) using two different approaches (1) using motion of curvature flow, and (2) from energy minimization.

For the motion due to curvature flow, we may set

$$(4) \qquad \vec{u} = -\sigma\kappa\vec{n} - [p]\vec{n}$$

where $\vec{u}$ is the velocity, $\sigma$ is the surface tension, $\kappa$ is the mean curvature, $\vec{n}$ is the outward normal vector at the front and $[p]$ is the jump of pressure across the interface. One assumption on our model is volume conservation through the motion. Consider the change of volume.

$$(5) \qquad Change\ of\ Volume = \int_{\partial\Omega} \vec{u} \cdot \vec{n} ds$$

$$= \int_{\partial\Omega} (-\sigma\kappa - [p]) ds$$

Equation(5) should equal to zero due to our volume constraint. This gives

$$(6) \qquad [p] = \frac{-\sigma \int_{\partial\Omega} \kappa ds}{\int_{\partial\Omega} ds} = -\sigma\bar{\kappa}$$

where $\kappa$ is the average curvature on the interface. Consider the level set $\phi = $ constant. Then the material derivative gives

(7)
$$\frac{D\phi}{Dt} = \frac{\partial\phi}{\partial t} + \vec{u} \cdot \nabla\phi = 0$$

Using equation (6) and (7), we arrive our governing equation using a distance function.

(8)
$$\frac{\partial\phi}{\partial t} = -\sigma(\kappa - \overline{\kappa})|\nabla\phi|$$

Now we move to the second approach. The energy of the surface of the solder joint without considering the gravitational energy is given by

(9)
$$E = \int_D \sigma\delta(\phi)|\nabla\phi|d\boldsymbol{x}$$

We want to minimize the surface energy with the volume conservation constraint:

(10)
$$\int_D H(D)d\boldsymbol{x} = constant \;\; in \;\; time$$

This is equivalent to find the minimum of the following functional:

(11)
$$f(\phi) = E + \lambda \int_D H(D)d\vec{\boldsymbol{x}} = constant \;\; in \;\; time$$

Using the variational level set approach by Zhao et al. [24], we can get the following minimization equation

(12)
$$\frac{\partial\phi}{\partial t} = -\sigma(\kappa + \lambda)|\nabla\phi| \quad in \quad D$$
$$\frac{\partial\phi}{\partial\vec{\boldsymbol{n}}} = 0 \quad on \quad \partial D$$

Then using a constraint(10), we can find $\lambda$.

(13)
$$\lambda = \frac{-\sigma \int_D \kappa\delta(\phi)|\nabla\phi|d\boldsymbol{x}}{\int_D \delta(\phi)|\nabla\phi|d\boldsymbol{x}} = -\overline{\kappa}$$

Substituting (13) into equation (12) gives us the same equation which we already derived above (eqn. (8)).

**2.2. Numerical Implementation.** Following is the outline of the numerical algorithm.
1. Initialize $\phi(\boldsymbol{x}, t)$ such that $\phi$ is a signed distance function to the interface.
2. Solve the governing equation using the method of lines, which means that splits the time and the space derivatives. For $\overline{\kappa}|\nabla\phi|$ term, we use a 2nd order ENO(Essentially Non-Oscillatory) scheme by Osher and Shu [16]. All derivatives of the term $\overline{\kappa}|\nabla\phi|$ are approximated by central differences. For the time derivative, we use 2nd order TVD(Total Variation Diminishing) type Runge-Kutta method [21].
3. Construct a new distance function by solving the following differential equation until the solution reaches a steady state near the front [22].

(14)
$$\frac{\partial\phi}{\partial t} = sign(\phi_0)(1 - |\nabla\phi|)$$

To eliminate the stiffness of sign function, we approximate $sign(\phi)$ by

$$(15) \qquad sign(\phi) = \frac{\phi}{\sqrt{\phi^2 + \epsilon^2}}$$

where $\epsilon$ is a very small number(e.g. $\epsilon = hx$ ).

4. We have now advanced one time step. Go to step 2 and repeat.

When our solution reaches steady state, then we should stop our calculation. As we are looking for a minimization solution, energy should decrease with time(i.e. $\frac{\partial E}{\partial t} \leq 0$) until we reach steady state. From this consideration, if $E_n \geq E_{n+1}$ , we may stop our calculation. Unfortunately in numerical computation this may not be true. In our experiment, we use following stopping criterion.

$$(16) \qquad \sum_{k=n-(2\alpha+1)}^{k=n-(\alpha+1)} E_k \geq \sum_{k=n-\alpha}^{k=n} E_k$$

Where $\alpha$ is an appropriate number(in our simulation, we use 10.) When we simulate the motion of the solder joint, merging or breaking will be the issue. Even though the level-set method takes care of those situations naturally (see Figure 1(b) ), we give some alteration to these cases because our equation includes local information(e.g. $\kappa$) depending on each level sets. For checking the case of merging, consider two distance functions $\phi_1$ and $\phi_2$ (see Figure 2 ). It shows that the merging region is region II which means two different level sets have a common region. The criterion for the case of merging using a level set notation is

$$(17) \qquad H(\phi_1(\boldsymbol{x})) \cdot H(\phi_2(\boldsymbol{x})) > 0.$$

In this case we assume that a single level set $\phi$ replaces the merged domain of the initial two level sets $\phi_1$ and $\phi_2$. The regenerated new level set $\phi$ satisfies the following condition:

$$(18) \qquad \phi = max(\phi_1, \phi_2)$$

After this procedure, we need to reinitialize a new level set $\phi$ to make sure that it is a distance function at least near the new interface. For both merging or breaking case, we can always check that the energy after the event is less than before: $(E_{after} \leq E_{before})$. The developed model can handle complicated pad geometry as shown in Figure 3.

## 3. Case Studies

In the following case studies, we will evaluate the impact of solder volume on joint quality. The optimal solder volume in a given package depends upon (1) geometrical variables such as pad geometry, pad dimension, pitch, number of joints, (2) process variables such as solder deposition thickness and its variation among the pad sites and reflow environment, and (3) assembly variables such as placement accuracy. The optimal solder volume is bounded by a lower and upper threshold. Solder volume deviating from the bounding limit will result in solder defect such as lack of solder joint formation or shorting of neighboring solder joints. The former is caused due to lack of sufficient solder at a given site and the later will be due to

excessive solder volume at a given site. In our case studies, we will establish analysis procedure for determining the bounding limit for a given assembly specification.

**3.1. Determining lower limit on solder volume to avoid defect.** The minimum solder volume that is required to present on a given pad site to avoid solder defect will depend on the design and process constraints imposed on a given assembly. Figure 4 shows three examples of assembly configuration for which we will determine the acceptable lower limit on solder volume to avoid joint defect. Figure 4-I shows an example of manipulating solder profile for better fatigue life. In this case, the goal is to determine the minimum acceptable solder volume to avoid solder joint separation. Figure 4-II shows the usage of large alignment/sacrificial joints that is provided at the four corners to ease the alignment between chip and the substrate and will act as the sacrificial joint that will take the load away from the inner joints. In this case, the goal is to determine the solder volume in the inner pads to ensure successful joint formation during reflow process. Figure 4-III represents the process deviation such as abnormal solder volume deposition at isolated site that can affect successful solder joint formation. In this case, the goal is to determine the acceptable maximum deviation in solder volume at a number of isolated pad sites that will allow successful joint formation.

As seen in Figure 4-I, the critical spacer gap beyond which the solder joint integrity is doubtful is a function of both design and process parameters. Consider a solder joint with top and bottom pads of 150 microns and a deposition height of 100 microns. For the present analysis, for simplicity we neglect the gravitational impact. We are interested in knowing the gap between the chip and substrate that will cause the joint to separate. Figure 5 shows a snapshot of sequence of event during the solder joint separation. As shown in Figure 6, the surface energy of the solder joint increases with gap height. However, the height can not be increased indefinitely as the solder joint's natural tendency to achieve minimum energy state. Beyond a critical height when the surface energy of the solder joint exceeds that of two separated bumps on chip/substrate pad sites, the joint will become unstable and will separate. The critical height is a function of (1) pad geometry, (2) solder volume and misalignment between top and bottom pads. For the given example, it can be seen that the critical height is reduced by 15 microns when the solder volume is reduced by 10%. To ensure defect free joint, one can take the spacer height to be about 50% of the lower limit on the critical height. In this case, it is about 118 microns.

Similar situation can also occur when significant deviation in solder volume take places at some random pad site(s). In this case, the goal is to determine how much deviation can be tolerated to ensure successful solder joint formation at that site. Figure 4-III shows the schematic representation of the proposed problem. The abnormal deviation is defined as the deviation that exceeds the specified process tolerance on the deposition thickness. The approach to solve this problem is to determine the critical gap between the chip and the substrate below which solder joint with a known volume will remain stable. Such information will be useful to the quality control personnel to decide whether to accept or reject the specific assembly component before the reflow process and to ensure that there is a reasonable chance of maintaining the joint integrity.

As a first step, the upper limit on the gap between chip and the substrate is determined. The required upper limit on the gap between the chip and the substrate is determined by (1) number of solder joints and their distribution, (2) vertical loading acting on the chip, (3) location of the site where the solder volume has

deviated beyond the specified process tolerance, and (4) substrate/chip deformation during the reflow process. Next, the lower limit on the solder volume that will allow successful joint formation is determined. The solder volume deviation is calculated as follows:

(1) for a given chip/substrate pad geometry determine the critical height of the solder joint - above which the joint will be unstable - as a function of deposition thickness and misalignment,

(2) for a given assembly specification - defined by pad geometry, distribution, vertical loading, and misalignment level - determine the maximum gap between chip and substrate when at least one solder joint located at an random site no longer supports the chip weight, and

(3) based on the result obtained from step 2 interpolate the result obtained in step 1 to arrive at the critical volume for that assembly configuration.

The critical gap is studied for the following assembly configuration. The chip and substrate pad geometry of the first assembly is circular with 100 micron diameter. The chip size is assumed to be 3.1 mm x 1.8 mm, the pad distribution is area-array (5 x 3) with total 15 joints, the pitch is assumed to be 500 microns. Figure 7 shows the maximum gap between the chip and the substrate supported by 14 joints (with 1 defect at a random site). In this case, the maximum gap is found to be one of the corner pad site. It also shows the critical height as a function of solder deposition height at the isolated pad site. The sequence of calculation to estimate the maximum acceptable deviation in solder volume is as follows: For a given solder deposition, drop a vertical line till it intersects the chip-substrate gap vs deposition height line. Then draw a horizontal line till it intersects the critical volume line. Then from that point of intersection draw another vertical line till it reaches the x-axis i.e. required limit on solder volume. It represents the maximum deviation in solder volume to create solder joint separation.

Figure 4-II represents another source of solder joint defect arises when the solder bump on chip/substrate can not come in contact to form a stable joint. This situation can be explained using the following case: consider a solder joint assembly with large alignment pads at the four corner of chip/substrate and small connector pads in the interior of chip/substrate. The function of the alignment pad is to allow large placement tolerance during assembly. The solder joints formed at the alignment pad sites carry the chip weight and aligns the chip with respect to the substrate. If the assembly is properly designed, the resultant gap between the chip and the substrate is enough to permit the smaller I/O bumps on the chip and the substrate to fuse and form stable solder joint. Figure 8 shows a snap shot of events leading to successful formation of a solder joint. During the initial phase of the assembly process, the alignment pads support the entire weight of the chip and determine the gap between the chip and substrate. Successful formation of inner joint will take place provided the gap and the misalignment level between the chip and the substrate will allow the solder bump on the chip and the substrate to make contact resulting successful joint formation.

Figure 9 shows the impact of misalignment and solder volume on minimum gap required for successful solder joint formation. The critical gap is studied for the following assembly: The chip and substrate pad geometry of the assembly is circular with 100 micron diameter. The chip size is assumed to be 3.1 mm x 1.8 mm, the pad distribution is area-array (5 x 3) with total 15 connector joints and 4 alignment joints. The pitch is assumed to be 250 microns. The alignment pad dimension is

200 microns diameter and pitch is 500 microns w.r.t. the neighboring connector pads.

**3.2. Determining upper limit on solder volume to avoid defect.** As we have noted earlier that solder volume when reached a lower threshold will create joint defect. Similarly, when solder reached an upper threshold, it will create another kind of solder defect such as joint shortening. The upper threshold is a function of pad geometry, size, chip weight, number of joints and pitch. Figure 10 shows one such example. With the tendency to incorporate larger number of I/O in an area-array format. One of the consequences is the reduction of pitch between the joints. This can give rise to potential defect due to merging of neighboring joints. This issue becomes critical when solder redistribution scheme is adopted to convert the peripheral distribution to area-array distribution. Because, the solder volume is not only affected by the pad geometry but also the connecting line dimension as the solder is deposited on it too during the deposition process (by using single mask for both defining the redistribution scheme as well as for the deposition process). Figure 10 shows a schematic representation of a pad redistribution scheme. It allows 44 peripheral I/O pads to be relocated in area-array fashion. The solder joint profile for such a scheme is shown in Figure 3. The goal is to determine the minimum acceptable pitch between the joint that will prevent joint shorting during the reflow process. Figure 11 shows a snap shot of joint shorting. Figure 12 shows critical pitch as a function of solder volume. The critical pitch refers to the minimum gap between neighboring joints to ensure no merging between the joints takes place. As expected for a given loading condition, the acceptable solder volume to avoid joint shorting decreases with decrease in joint pitch. For redistribution scheme shown in Figure 10, where the solder volume not only depends on pad size but also on the connecting line, determining the maximum acceptable line length will be a function of joint pitch.

## 4. Summary and conclusion

A level-set approach to solder joint profile model has been developed. This is used to predict joint profile under two conditions: (1) joint separation, and (2) joint shorting. The model was used later to check the joint quality for a specific set of assembly configuration. No attempt has been made to obtain a more generic result. We intend to study a more generic case in the future.
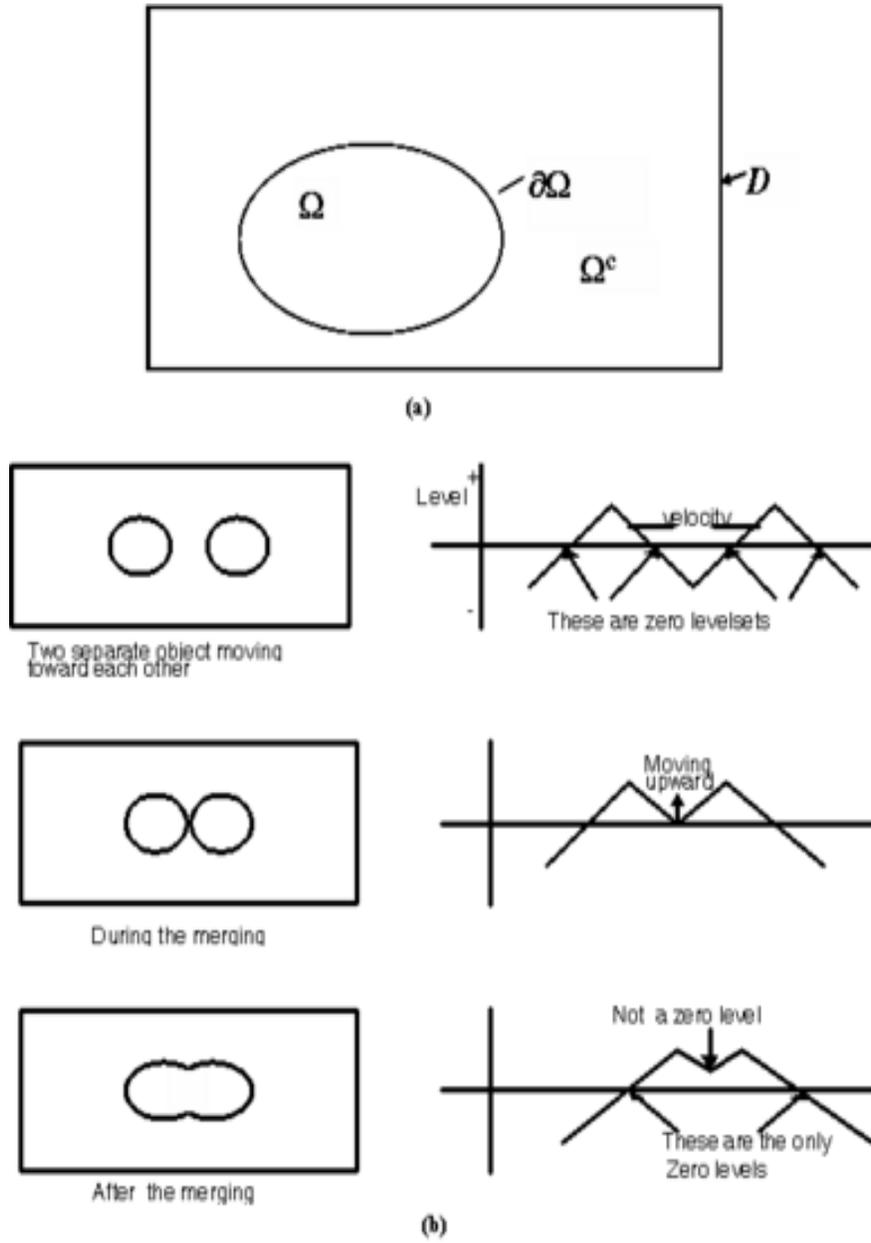
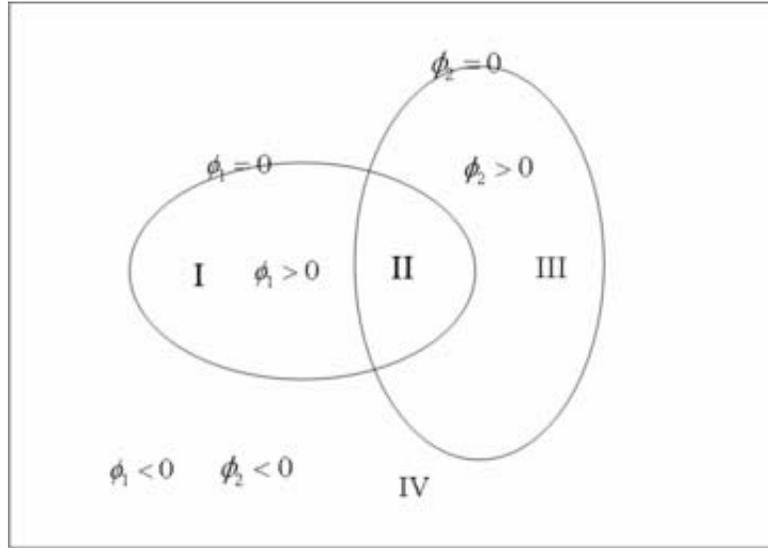FIGURE 1.  (a)Domain for the levelset (b)concept of merging and separation in levelset

FIGURE 2.   Computational domain representing merging of interfaces
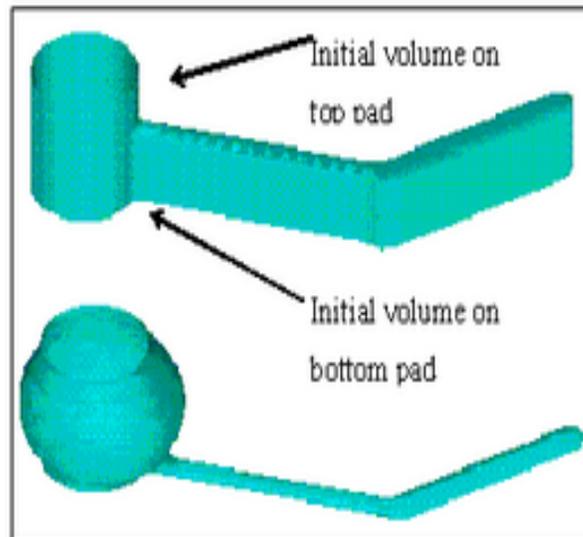


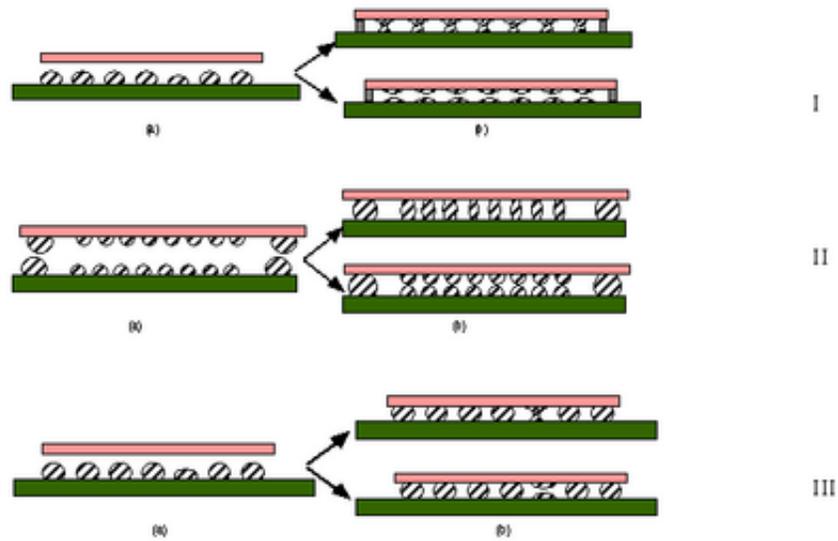FIGURE 3.   Initial and final profile of a solder joint with irregular boundary

FIGURE 4. Schematic representation of possible source of solder defect. (I)manipulation of solder profile for better fatigue-life, (II) solder reflow process with large alignment bumps and small connector bumps for reducing alignment requirement or to form sacrificial solder joint, and (III) possible solder defect due to abnormal solder deposition at isolated pad sites.
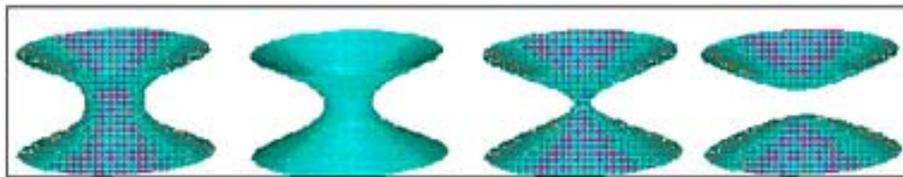


FIGURE 5. Sequence of events associated with unstable solder profile with circular pad geometry (100 x 100 microns)
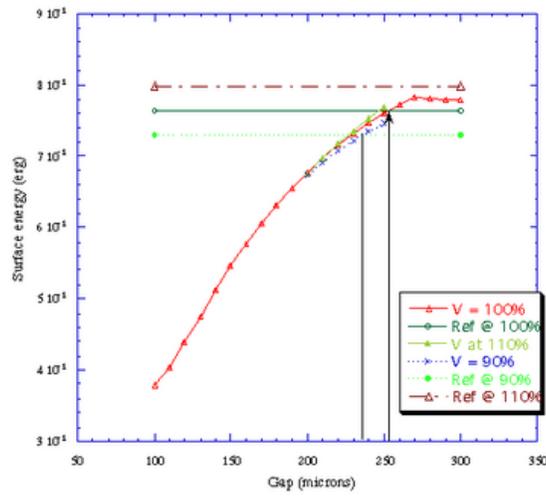
FIGURE 6.   Condition for solder joint separation - Limits for joint separation under minimum energy assumption. ( V: the volume of solder)
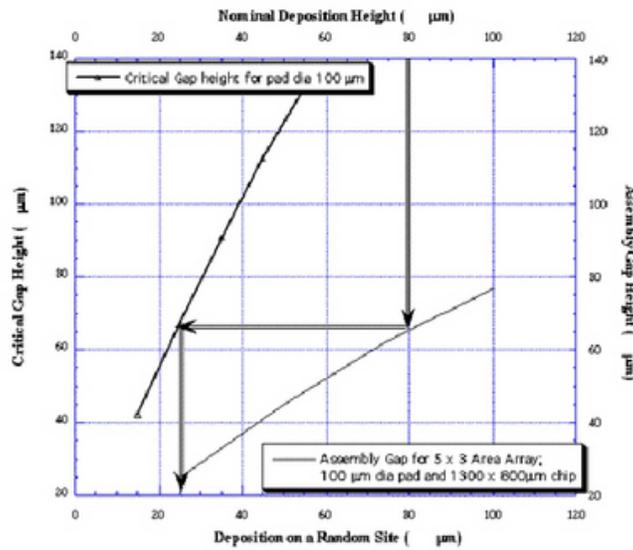


FIGURE 7.   Determine (i) critical height as a function of deposited solder thickness and pad geometry, (ii) gap between chip and substrate as a function of solder deposition height in all pads except for the isolated site, and (iii) interpolate to determine the upper limit of the solder volume deviation at an isolated site for a stable profile.
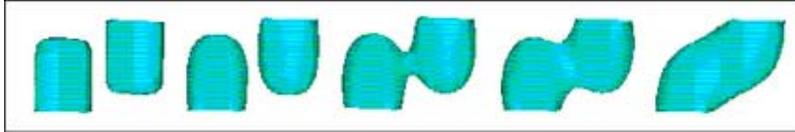
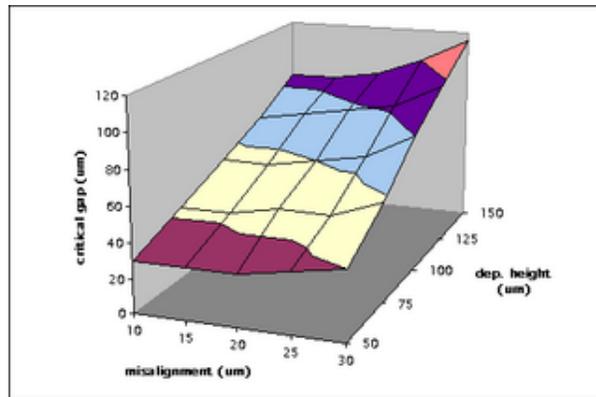Figure 8.   Snapshot of sequence of events leading to a successful solder joint formation.



Figure 9.   Critical gap between chip and substrate required for successful formation of solder joint. It is assumed that both chip and substrate contains equal amount of solder at the pad site.
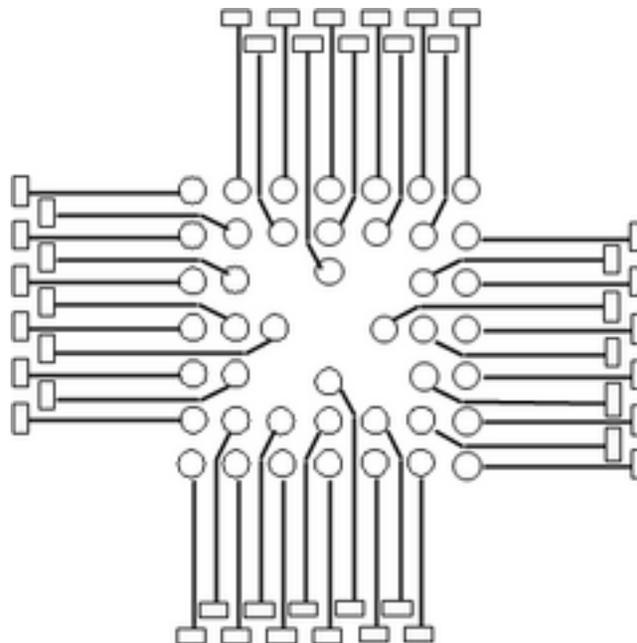


Figure 10.   Schematic view of pad redistribution converting the peripheral distribution to area-array distribution.
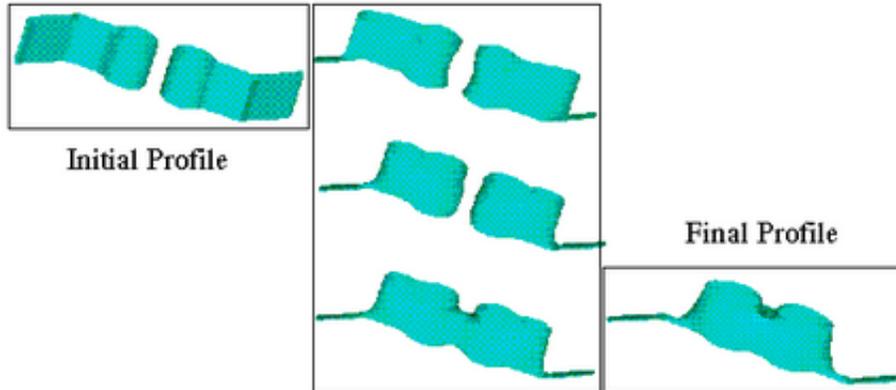
FIGURE 11.   Snap shot of sequence of events leading to the defect
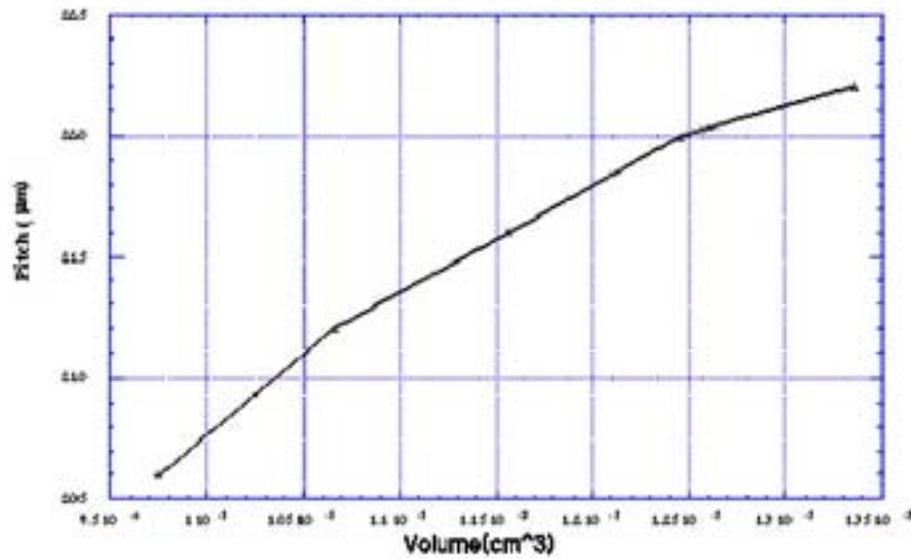due to merger of two neighboring joints.



FIGURE 12.   Critical pitch as a function of solder volume to avoid shorting

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